NB638

High Efficiency, Fast Transient, 7A, 28V nchronous Step-down Converter in a Tiny 3x4mm QFN Package

The Future of Analog IC Technology®

DESCRIPTION

The NB638 is a fully integrated, high frequency synchronous rectified step-down switch mode converter. It offers a very compact solution to achieve 7A continuous output current over a wide input supply range with excellent load and line regulation. The NB638 operates at high efficiency over a wide output current load range.

Constant-On-Time (COT) control mode provides fast transient response and eases loop stabilization.

Full protection features include SCP, OCP, OVP, UVP and thermal shutdown.

The NB638 requires a minimum number of readily available standard external components and is available in a space-saving QFN20 (3x4mm) package.

FEATURES

- Wide 4.5V to 28V Operating Input Range
- 7A Output Current
- Internal 30mΩ High-Side, 12mΩ Low-Side Power MOSFETs
- Proprietary Switching Loss Reduction Technique
- 1% Reference Voltage
- Programmable Soft Start Time
- Soft Shutdown
- 200kHz to 1MHz Switching Frequency
- SCP, OCP, OVP, UVP Protection and Thermal Shutdown
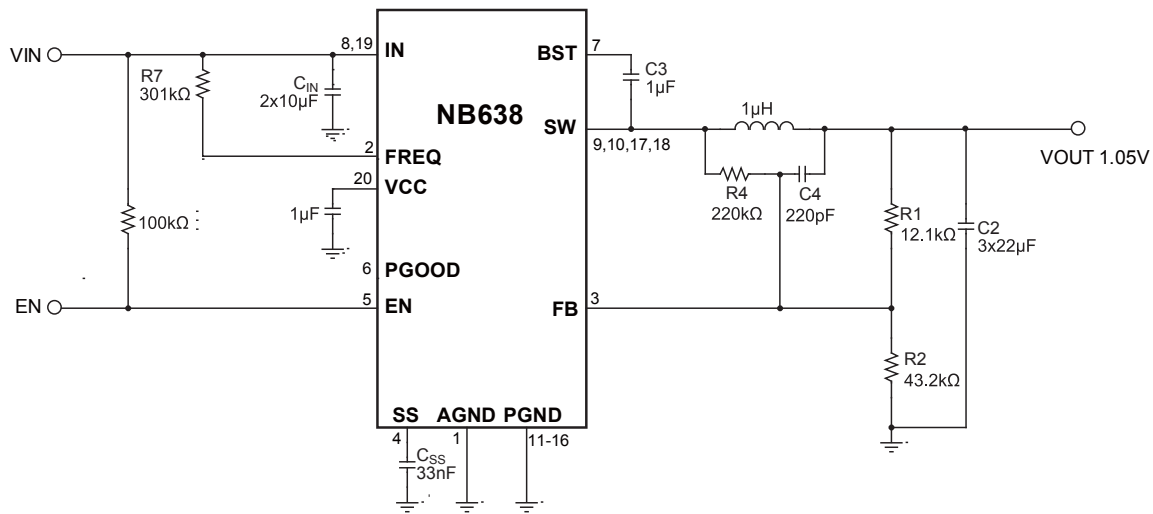- Output Adjustable from 0.8V to 13V
- Available in a QFN20 (3x4mm) Package

APPLICATIONS

- Notebook Systems and I/O Power
- Networking Systems
- Optical Communication Systems
- Distributed Power and POL Systems

TYPICAL APPLICATION

ORDERING INFORMATION

Part Number*	Package	Top Marking
NB638DL	QFN20 (3x4mm)	NB638

* For Tape & Reel, add suffix –Z (e.g. NB638DL–Z)
For RoHS compliant packaging, add suffix –LF (e.g. NB638DL–LF–Z)

PACKAGE REFERENCE

TOP VIEW

EXPOSED PAD
ON BACKSIDE
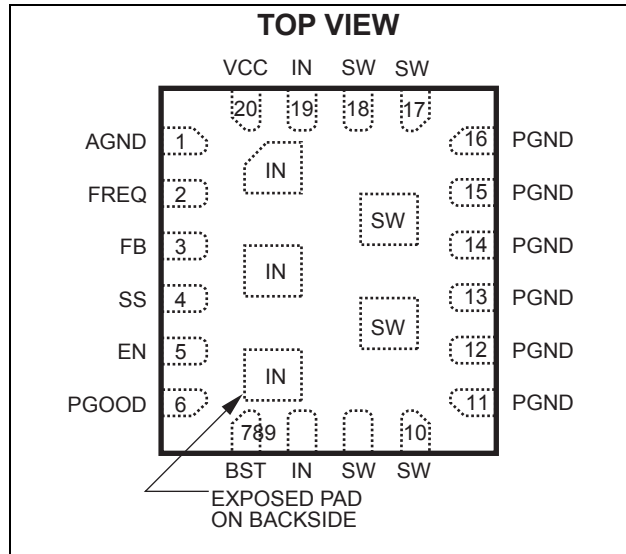
ABSOLUTE MAXIMUM RATINGS [1]

Supply Voltage V_{IN} 30V
V_{SW} .... -0.3V to V_{IN} + 0.3V
V_{BST} .... V_{SW} + 6V
$I_{VIN (RMS)}$ 3.5A
V_{PGOOD} .... -0.3V to V_{CC}+0.6V
All Other Pins .... -0.3V to +6V
Continuous Power Dissipation (T_A = +25°C) [2]
……………………………………… ……………2.6W
Junction Temperature .... 150°C
Lead Temperature .... 260°C
Storage Temperature .... -65°C to +150°C

Recommended Operating Conditions [3]

Supply Voltage V_{IN} .... 4.5V to 28V
Output Voltage V_{OUT} .... 0.8V to 13V
Maximum Junct. Temp (T_J) ...... -40°C to +125°C

Thermal Resistance [4] θ_{JA} θ_{JC}

QFN20 (3x4mm) .... 48 ...... 10 ... °C/W

Notes:
1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_A = +25°C, unless otherwise noted.

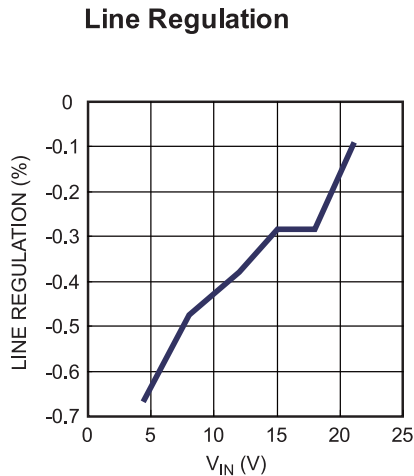| Parameters Sy	mbol	Condition	Min	Typ	Max	Units
Supply Current (Shutdown)	I_{IN} V	$_{EN}$ = 0V		0		µA
Supply Current (Quiescent)	I_{IN}	V_{EN} = 2V V_{FB} = 1V	500			µA
HS Switch On Resistance [5] HS	RDS-ON			30		mΩ
LS Switch On Resistance [5] LS	RDS-ON			12		mΩ
Switch Leakage	SW$_{LKG}$	V_{EN} = 0V V_{SW} = 0V or 12V	0		10	µA
Current Limit	I_{LIMIT}			12		A
One-Shot On Time	T_{ON}	R7=301kΩ V_{OUT}=1.2V	250			ns
Minimum Off Time[5] T	OFF			100		ns
Fold-back Off Time[5]	T_{FB}	I_{LIM}=1(HIGH)		1.4		µs
OCP hold-off time[5] T	OC	I_{LIM}=1(HIGH)			40	µs
Feedback Voltage	V_{FB}	T_A=25°C	807 815		823	mV
		0°C <T_A<70°C	803 815		827	
Feedback Current	I_{FB}	V_{FB} = 815mV		10	50	nA
Soft Start Charging Current	I_{SS}	V_{SS}=0V		8.5		µA
Soft Stop Charging Current	I_{SS}	V_{SS}=0.815V		8.5		µA
Power Good Rising Threshold	PGOOD$_{Vth-Hi}$			0.9		V_{FB}
Power Good Falling Threshold	PGOOD$_{Vth-Lo}$			0.85		V_{FB}
Power Good Rising delay	T_{PGOOD}	T_{SS}=1ms		1		ms
Power Good Rising delay	T_{PGOOD}	T_{SS} =2ms		1.5		ms
Power Good Rising delay	T_{PGOOD}	T_{SS} =3ms		2		ms
EN Rising Threshold	EN$_{Vth-Hi}$		1.05	1.35	1.60	V
EN Threshold Hysteresis	EN$_{Vth-Hys}$		250	420	550	mV
EN Input Current	I_{EN}	V_{EN} = 2V		2		µA
V_{IN} Under-Voltage Lockout Threshold Rising	INUV$_{Vth}$		3.8	4.0	4.2	V
V_{IN} Under-Voltage Lockout Threshold Hysteresis	INUV$_{HYS}$			880		mV
V_{CC} Regulator	V_{CC}			5		V
V_{CC} Load Regulation		I_{CC}=5mA		5		%
Vo Over-Voltage Protection Threshold	V_{OVP}			1.25		V_{FB}
Vo Under-Voltage Detection Threshold	V_{UVP}			0.7		V_{FB}
Thermal Shutdown	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{SD-HYS}			25		°C

Note:
5) Guaranteed by design.

PIN FUNCTIONS

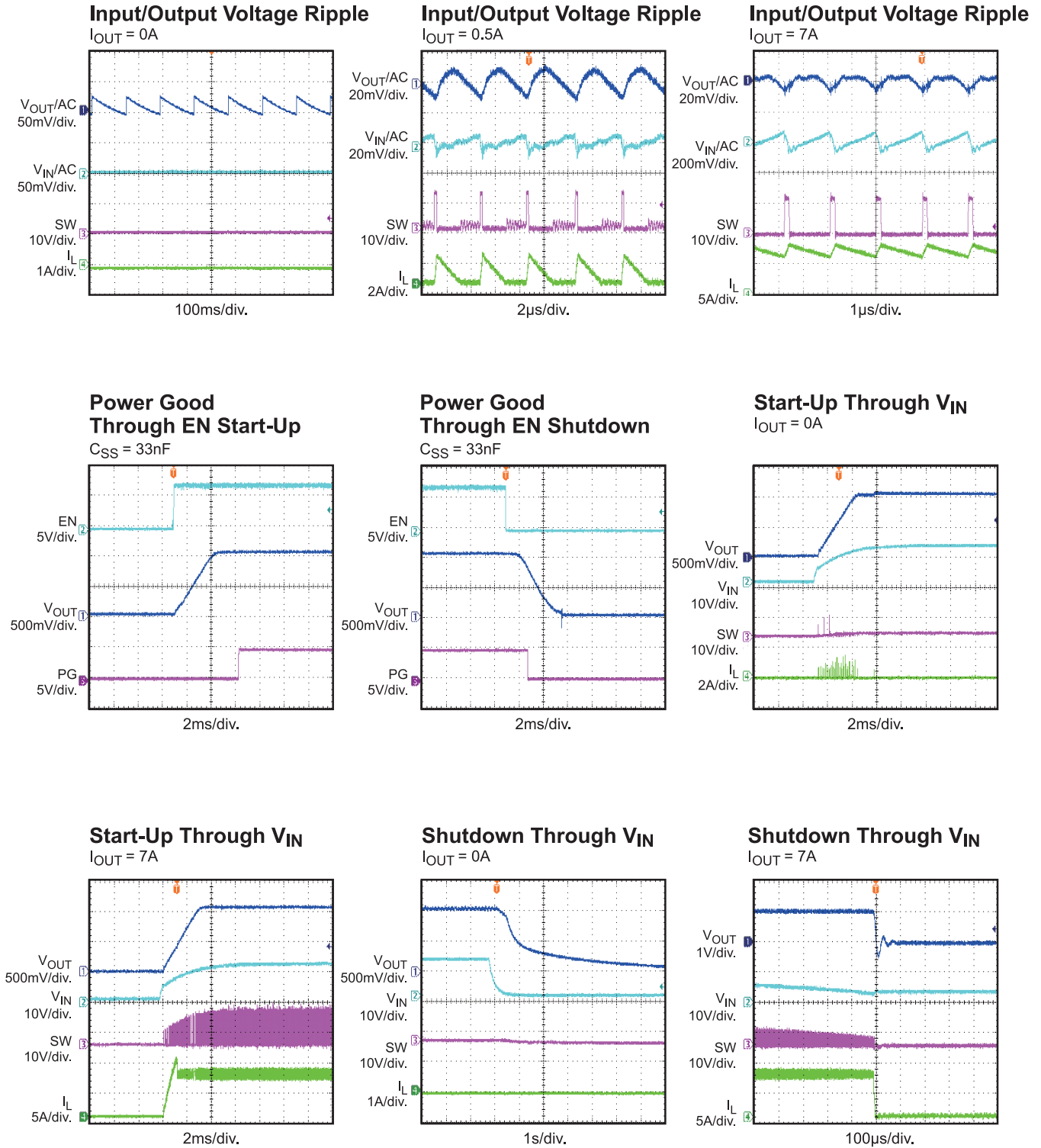| Pin #	Name	Description
1 AGND		Analog Ground.
2 FREQ		Frequency Set during CCM operation. The ON period is determined by the input voltage and the frequency-set resistor connected to FREQ pin. Connect a resistor to IN for line feed-forward. Decouple with a 1nF capacitor.
3 FB		Feedback. An external resistor divider from the output to GND, tapped to the FB pin, sets the output voltage.
4 SS		Soft Start. Connect an external SS capacitor to program the soft start time for the switch mode regulator. When the EN pin becomes high, an internal current source (8.5µA) charges up the SS capacitor and the SS voltage slowly ramps up from 0 to V_{FB} smoothly. When the EN pin becomes low, an internal current source (8.5µA) discharges the SS capacitor and the SS voltage slowly ramps down.
5 EN		EN=1 to enable the NB638. For automatic start-up, connect EN pin to IN with a 100kΩ resistor. It includes an internal 1MΩ pull-down resistor.
6	PGOOD	Power Good Output. The output of this pin is an open drain and is high if the output voltage is higher than 90% of the nominal voltage. There is delay from FB ≥ 90% to PGOOD high, which is 50% of SS time plus 0.5ms.
7 BST		Bootstrap. A 0.1µF-1µF capacitor connected between SW and BS pins is required to form a floating supply across the high-side switch driver.
8, 19	IN	Supply Voltage. The NB638 operates from a +4.5V to +28V input rail. C_{IN} is needed to decouple the input rail. Use wide PCB traces and multiple vias to make the connection.
9, 10, 17, 18	SW	Switch Output. Use wide PCB traces and multiple vias to make the connection.
11-16 PGND		System Ground. This pin is the reference ground of the regulated output voltage. For this reason care must be taken in PCB layout.
20 VCC		Internal Bias Supply. Decouple with a 1µF capacitor as close to the pin as possible.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN}=12V, V_{OUT} =1.05V, L=1µH, T_A=+25°C, unless otherwise noted.

Efficiency vs. Load Current
F_{SW} =500kHz

Efficiency vs. Load Current
V_{OUT}=5V, F_{SW} =500kHz, L=3.3µH

V_{CC} Regulator Line Regulation

Line Regulation

Load Regulation

Case Temperature Rise vs. Output Current
T_{case}=22.6°C

Frequency vs. Temperature
I_{OUT}=7A

Frequency vs. V_{IN}
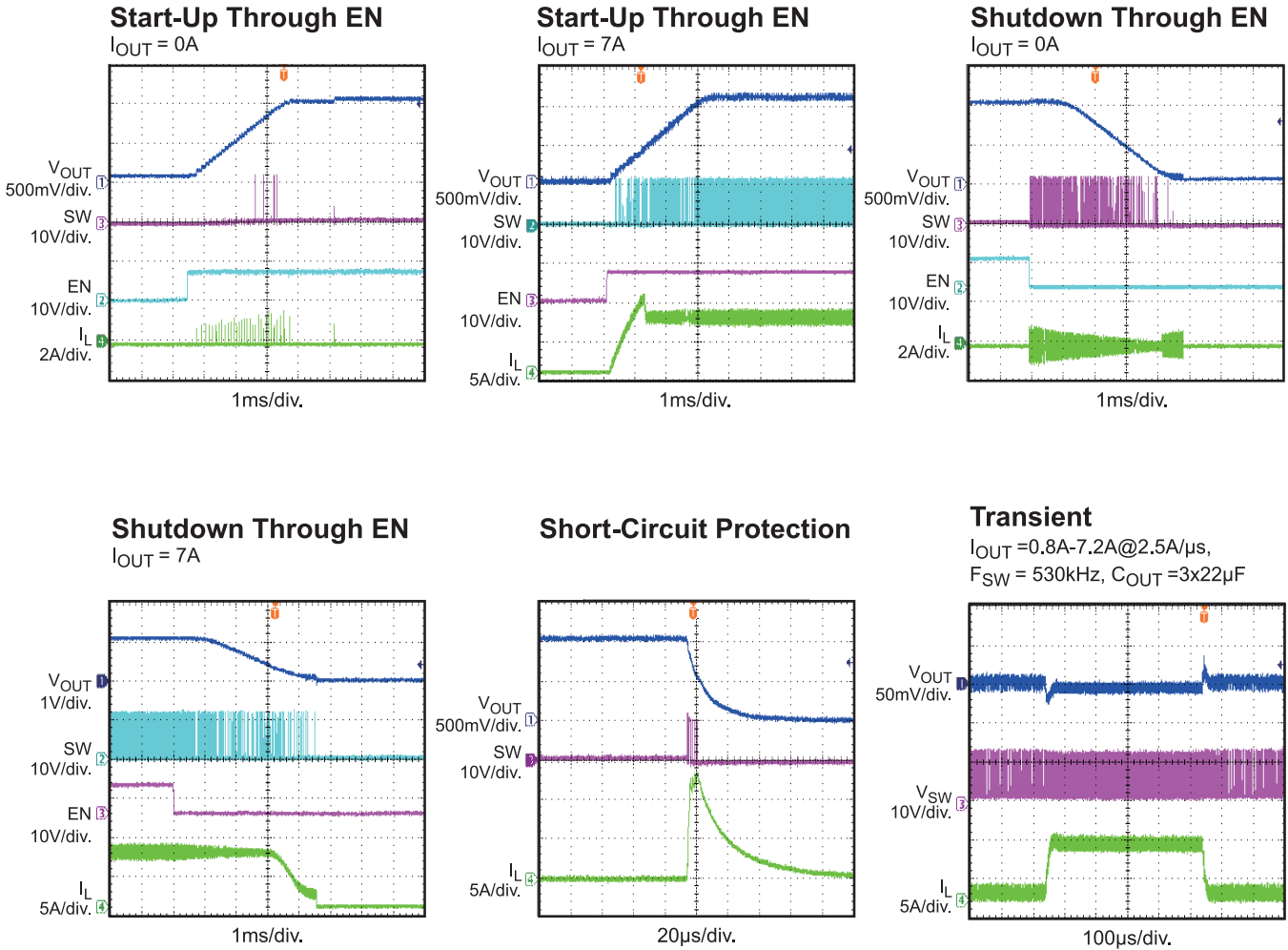$R_{F_{SW}}$=174kΩ, I_{OUT}=7A

Frequency vs. Load Current

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=12V, V_{OUT} =1.05V, L=1µH, T_A=+25°C, unless otherwise noted.

Input/Output Voltage Ripple
I_{OUT} = 0A

Input/Output Voltage Ripple
I_{OUT} = 0.5A

Input/Output Voltage Ripple
I_{OUT} = 7A

Power Good
Through EN Start-Up
C_{SS} = 33nF

Power Good
Through EN Shutdown
C_{SS} = 33nF

Start-Up Through V_{IN}
I_{OUT} = 0A

Start-Up Through V_{IN}
I_{OUT} = 7A

Shutdown Through V_{IN}
I_{OUT} = 0A

Shutdown Through V_{IN}
I_{OUT} = 7A

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

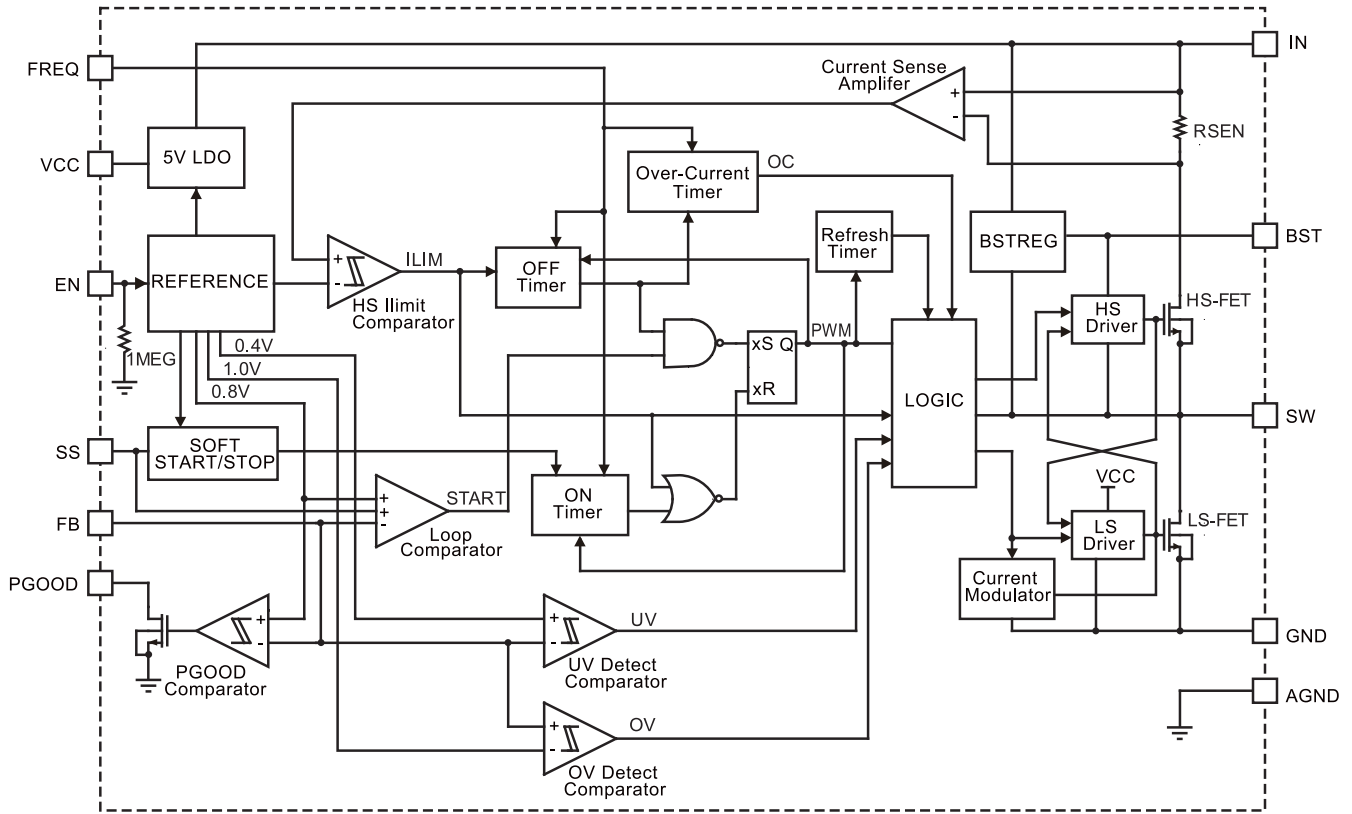V_{IN}=12V, V_{OUT} =1.05V, L=1µH, T_A=+25°C, unless otherwise noted.

Start-Up Through EN
I_{OUT} = 0A

V_{OUT} 500mV/div.
SW 10V/div.
EN 10V/div.
I_L 2A/div.

1ms/div.

Start-Up Through EN
I_{OUT} = 7A

V_{OUT} 500mV/div.
SW 10V/div.
EN 10V/div.
I_L 5A/div.

1ms/div.

Shutdown Through EN
I_{OUT} = 0A

V_{OUT} 500mV/div.
SW 10V/div.
EN 10V/div.
I_L 2A/div.

1ms/div.

Shutdown Through EN
I_{OUT} = 7A

V_{OUT} 1V/div.
SW 10V/div.
EN 10V/div.
I_L 5A/div.

1ms/div.

Short-Circuit Protection

V_{OUT} 500mV/div.
SW 10V/div.
I_L 5A/div.

20µs/div.

Transient
I_{OUT} =0.8A-7.2A@2.5A/µs,
F_{SW} = 530kHz, C_{OUT} =3x22µF

V_{OUT} 50mV/div.
V_{SW} 10V/div.
I_L 5A/div.

100µs/div.

BLOCK DIAGRAM

Figure 1—Functional Block Diagram

OPERATION

PWM Operation

The NB638 is a fu lly integrated synchronous rectified step-down switch mode converter. Constant-on-time (COT) control is employed t o provide fast transient r esponse an d easy loo p stabilization. At the beginning of ea ch cycle, th e high-side MOSFET (HS-FET) is tur ned ON wh en the feedback voltage (V_{FB}) is below the reference voltage (V_{REF}), which in dicates insufficient output voltage. The ON period is deter   mined by the input voltag e and the f requency-set resist or a s follows:

$$T_{ON}(s) = \frac{6 \times R7(k)}{V_{IN}() - 0.4} + 40(ns) \qquad (1)$$

After the ON period elapses, the HS-FET is turned off, or becomes OFF state. It is turned ON again when V_{FB} drops below V_{REF}. By repeating operation th is way, the converter r egulates th e output voltage. The inte grated low-side MOSFET (LS-FET) is turned on w hen the HS-FET is in it s OFF state to minimize the conduction loss. The re will be a de ad short be tween input and GND i f both HS-FET and LS-FET are turned on at th e same time. It's calle d shoot-through. In order to avoid shoot-through, a dead-time (DT) is internally generated between HS-FET off and LS-FET on, or LS-FET off and HS-FET on.
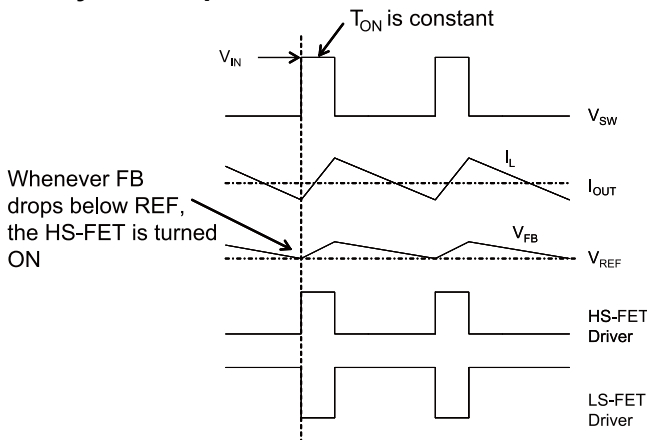
Heavy-Load Operation

Figure 2—Heavy Load Operation

As Figure 2 shows, when the outp ut current is high, the HS-FET and LS-FET repeat on/off as described a bove. In this operation, the inducto r current will never go to zero. It's calle d continuous-conduction-mode (CCM) operation. In CCM operation, the switching frequ ency (F_{SW}) is fairly constant.

Light-Load Operation

At light loa d or no lo ad conditio n, the outp ut drops very slowly and the NB638 reduces the switching fr equency automatically to maintain high efficiency. The light load operation is show n in Figure 3. The V_{FB} d oes not rea ch V_{REF} when the inductor current is approaching zero. The LS-FET driver t urns into tri-state (high Z) wheneve r the inducto r current reaches zer o. A current modulator takes over the control o f LS-FET and limits the inductor cur rent to le ss than -1m A. Hence, the output capa citors discharge slowly to GND throug h LS-FET. As a result, the efficiency at light load condition is greatly improved. At light load condit ion, the HS-FET is not t urned ON as frequently as at heavy load condition. This is called skip mode.
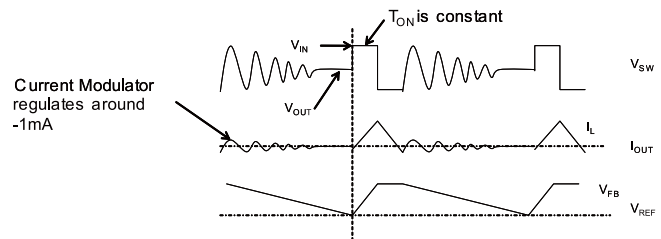

Figure 3—Light Load Operation

As the output current increases from the lig ht load condition, the time period within which t he current modulator regulates beco   mes shorter. The HS-FET is t   urned ON more frequently. Hence, th e switchin g frequen cy increases correspondingly. The output curren t reaches th e critical level when the current modulator time is zero. The critical level of the outp ut current is determined as follows:

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2L \times F_{SW} \times V_{IN}} \qquad (2)$$

It turns into PWM mode once the output current exceeds the critical level. After that, the switching frequency stays fairly constant over the output current range.

Switching Frequency

Constant on-time (COT) control is used in the NB638 and there is no dedicated oscillator in the IC. The input voltage is feed-forwarded to the on-time one-shot timer through the resistor R7. The duty ratio is kept as V_{OUT}/V_{IN}. Hence, the switching frequency is fairly constant over the input voltage range. The switching frequency can be set as follows:

$$F_{SW}(kHz) = \frac{10^6}{6 \times R7(k) \times \frac{V_{IN}(V)}{V_{IN}(V) - 0.4} \times \frac{1}{V_{OUT}(V)} + T_{DELAY}(ns)} \quad (3)$$

Where T_{DELAY} is the comparator delay. It's about 40ns.

Frequency vs. R_{FREQ}
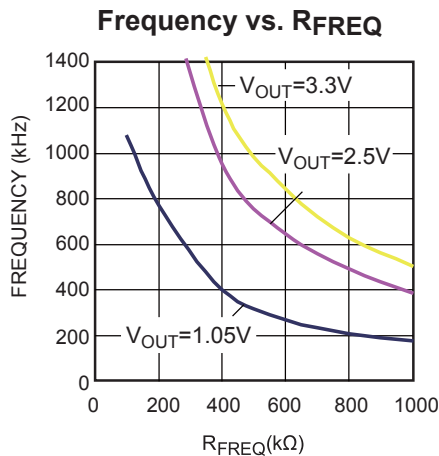
Generally, the NB638 is set for 200 kHz to 1MHz application. It is optimized to operate at high switching frequency with high efficiency. High switching frequency makes it possible to utilize small sized LC filter components to save system PCB space.

Jitter and FB Ramp Slope

Figure 4 and Figure 5 show jitter occurring in both PWM mode and skip mode. When there is noise in the V_{FB} downward slope, the ON time of HS-FET deviates from its intended location and produces jitter. It is necessary to understand that there is a relationship between a system's stability and the steepness of the V_{FB} ripple's downward slope. The slope steepness of the V_{FB} ripple dominates in noise immunity. The

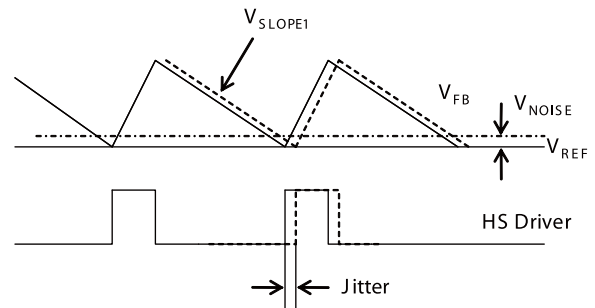magnitude of the V_{FB} ripple doesn't directly affect the noise immunity directly.
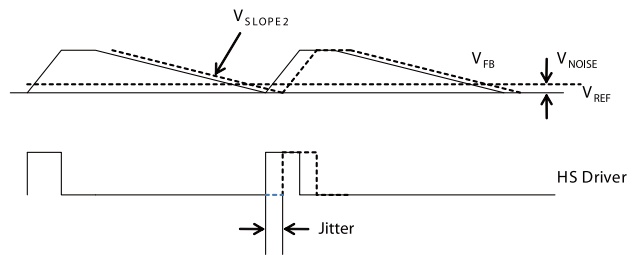

Figure 4—Jitter in PWM Mode

Figure 5—Jitter in Skip Mode

Ramp with Large ESR Cap

In the case of POSCAP or other types of capacitor with larger ESR is applied as output capacitor. The ESR ripple dominates the output ripple, and the slope on the FB is quite ESR related. Figure 6 shows an equivalent circuit in PWM mode with the HS-FET off and without an external ramp circuit. Turn to application information section for design steps with large ESR caps.
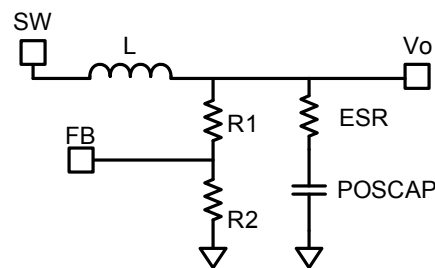

Figure 6—Simplified Circuit in PWM Mode without External Ramp Compensation

To realize the stability when no external ramp is used, usually the ESR value should be chosen as follow:

$$R_{ESR} \geq \frac{\frac{T_{SW}}{0.7 \times \pi} + \frac{T_{ON}}{2}}{C_{OUT}} \quad (4)$$

Tsw is the switching period.

Ramp with small ESR Cap

When the output capacitors are ceramic ones, the ESR ripple is not high enough to stabilize the system, and external ramp compensation is needed. Skip to application information section for design steps with small ESR caps.
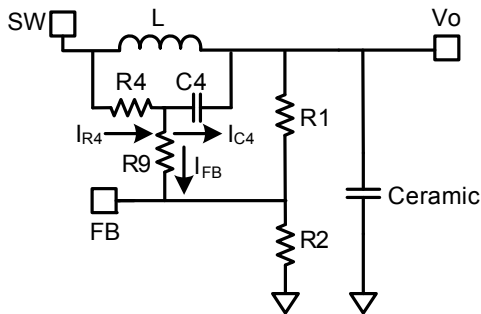

Figure 7—Simplified Circuit in PWM Mode with External Ramp Compensation

In PWM mode, an equivalent circuit with HS-FET off and the use of an external ramp compensation circuit (R4, C4) is simplified in Figure 7. The external ramp is derived from the inductor ripple current. If one chooses C4, R9, R1 and R2 to meet the following condition:

$$\frac{11}{2\pi \times F_{SW} \times C_4} << \frac{1}{5} \left(\frac{R_1 \times R_2}{R_1 + R_2} + R_9 \right) \quad (5)$$

Where:

$$I_{R4} = I_{C4} + I_{FB} \approx I_{C4} \quad (6)$$

And the ramp on the V_{FB} can then be estimated as:

$$V_{RAMP} = \frac{V_{IN} - V_O}{R_4 \times C_4} \times T_{ON} \times \frac{R_1 // R_2}{R_1 // R_2 + R_9} \quad (7)$$

The downward slope of the V_{FB} ripple then follows

$$V_{SLOPE1} = \frac{-V_{RAMP}}{T_{off}} = \frac{-V_{OUT}}{R_4 \times C_4} \quad (8)$$

As can be seen from equation 8, if there is instability in PWM mode, we can reduce either R4 or C4. If C4 can not be reduced further due to

limitation from equation 5, then we can only reduce R4. For a stable PWM operation, the V_{slope1} should be design follow equation 9.

$$-V_{slope1} \geq \frac{\frac{T_{SW}}{0.7 \times \pi} + \frac{T_{ON}}{2} - R_{ESR} C_{OUT}}{2k \times C_{OUT}} V_{OUT} + \frac{Io \times 10^{-3}}{T_{SW} - T_{on}} \quad (9)$$

Io is the load current.

In skip mode, the downward slope of the V_{FB} ripple is almost the same whether the external ramp is used or not. Fig.9 shows the simplified circuit of the skip mode when both the HS-FET and LS-FET are off.
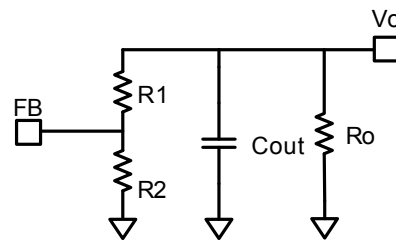

Figure 8—Simplified Circuit in skip Mode

The downward slope of the V_{FB} ripple in skip mode can be determined as follow:

$$V_{SLOPE2} = \frac{-V_{REF}}{((R_1 + R_2) // Ro) \cdot C_{OUT}} \quad (10)$$

Where Ro is the equivalent load resistor. As described in Fig.5, V_{SLOPE2} in the skip mode is lower than that is in the PWM mode, so it is reasonable that the jitter in the skip mode is larger. If one wants a system with less jitter during ultra light load condition, the values of the V_{FB} resistors should not be too big, however, that will decrease the light load efficiency.

Soft Start/Stop

The NB638 employs soft start/stop (SS) mechanism to ensure smooth output during power-up and power shutdown. When the EN pin becomes high, an internal current source (8.5 µA) charges up the SS CAP. The SS CAP voltage takes over the REF voltage to the PWM comparator. The output voltage smoothly ramps

up with the SS voltage. Once the SS voltage reaches the same level as the REF voltage, it keeps ramping up while V_{REF} takes over the PWM comparator. At this point, the soft start finishes and it enters into steady state operation.

When the EN pin becomes low, the SS CAP voltage is discharged through an 8.5 µA internal current source. Once the SS voltage reaches REF voltage, it takes over the PWM comparator.

The output voltage will decrease smoothly with SS voltage until zero level. The SS Cap value can be determined as follows:

$$C_{SS}(F) = \frac{T_{SS}(s) \times I_{SS}(\mu A)}{V_{REF}(V)} \qquad (11)$$

If the output capacitors have large capacitance value, it's not recommended to set the SS time too small. Otherwise, it's easy to hit the current limit during SS. A minimum value of 4.7nF should be used if the output capacitance value is larger than 330µF.

Power Good (PGOOD)

The NB638 has power-good (PGOOD) output. The PGOOD pin is the open drain of a MOSFET. It should be connected to V_{CC} or other voltage source through a resistor (e.g. 100k). After the input voltage is applied, the MOSFET is turned on so that the PGOOD pin is pulled to GND before SS is ready. After FB voltage reaches 90% of REF voltage, the PGOOD pin is pulled high after a delay.

The PGOOD delay time is determined as follows:

$$T_{PGOOD}(ms) = 0.5 \times T_{SS}(ms) + 0.5 \qquad (12)$$

When the FB voltage drops to 85% of REF voltage, the PGOOD pin will be pulled low.

Over-Current Protection (OCP) and Short-Circuit Protection (SCP)

The NB638 has cycle-by-cycle over-current limit control. The inductor current is monitored during the ON state. Once it detects that the inductor current is higher than the current limit, the HS-

FET is turned off. At the same time, the OCP timer is started. The OCP timer is set as 40 µs. If in the following 40 µs, the current limit is hit for every cycle, then it'll trigger OCP latch-off. The converter needs power cycle to restart after it triggers OCP.

If short circuit happens, then the current limit will be hit immediately and the FB voltage will become lower than 50% of the REF voltage. When the current limit is hit and the FB voltage is lower than 50% of the REF voltage (0.815V), the device considers this as a dead short on the output and triggers SCP latch-off immediately. This is short circuit protection (SCP).

Over/Under-voltage Protection (OVP/UVP)

The NB638 monitors the output voltage through a resistor divider feedback (FB) voltage to detect overvoltage and undervoltage on the output. When the FB voltage is higher than 125% of the REF voltage (0.8V), it'll trigger OVP latch-off. Once it triggers OVP, the LS-FET is always on while the HS-FET is always off. It needs power cycle to power up again. When the FB voltage is below 50% of the REF voltage (0.815V), it is recognized as UV (under-voltage). Usually, UVP accompanies a hit in current limit and results in SCP.

UVLO protection

The NB638 has under-voltage lock-out protection (UVLO). When the input voltage is higher than the UVLO rising threshold voltage, the NB638 will be powered up. It shuts off when the input voltage is lower than the UVLO falling threshold voltage. This is non-latch protection.

Thermal Shutdown

Thermal shutdown is employed in the NB638. The junction temperature of the IC is internally monitored. If the junction temperature exceeds the threshold value (typically 150ºC), the converter shuts off. This is a non-latch protection. There is about 25ºC hysteresis. Once the junction temperature drops to about 125ºC, it initiates a SS.

APPLICATION INFORMATION

Setting the Output Voltage-Large ESR Caps

For applications that electrolytic capacitor or POS capacitor with a controlled output o f ESR is set as output capacitors. The output voltage is set by feedback resistors R1 and R2. As figure 9 shows.
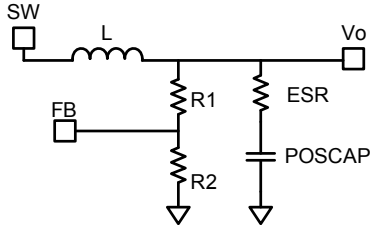

Figure 9—Simplified Circuit of POS Capacitor

First, choo se a value for R2. R2 should be chosen rea sonably, a small R2 will lead to considerable quiescent current lo ss while to o large R2 makes the FB noise sensitive. It is recommended to choo se a value within 5k Ω-50kΩ for R 2, using a comparatively larger R2 when Vout is low, etc., 1.05V, and a smaller R2 when Vout is high. Th en R1 is d etermined as follow with the output ripple considered:

$$RR_1 = \frac{V_{OUT} - \frac{1}{2}\Delta V_{OUT} - V_{REF}}{V_{REF}} \quad (13)$$

ΔV_{OUT} is the output ripple determined by equation 21.

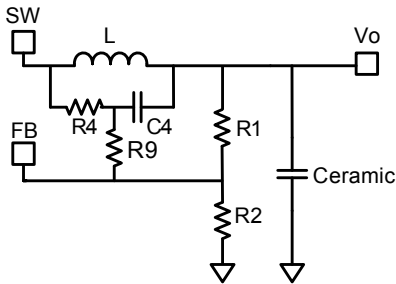### Setting the Output Voltage-Small ESR Caps

Figure 10—Simplified Circuit of Ceramic Capacitor

When low ESR ceramic capacitor is used in the output, an external voltage ramp should be added to FB through resistor R4 and capacit or C4.The output voltage is influenced by ramp voltage V $_{RAMP}$ beside s R divider as shown in figure 11. The V$_{RAMP}$ can be calculated as shown

in equation 7. R2 should be chosen reasonably, a small R2 will lead t o considera ble quiesce nt current loss while too large R2 makes the F B noise sensit ive. It is recommended to choose a value within 5k Ω-50kΩ for R2 , using a comparatively larger R2 when Vo is low, etc.,1.05V, and a smaller R2 when Vo is high . And the value of R1 then is determined as follow:

$$R_1 = \frac{R_2}{\frac{V_{FB(AVG)}}{(V_{OUT} - V_{FB(AVG)})} - \frac{R_2}{R_4 + R_9}} \quad (14)$$

The V $_{FB(AVG)}$ is the average value on the F B, $V_{FB(AVG)}$ varies with t he Vin, Vo, and load condition, etc., its value on the skip mode would be lower th an that of the PWM mode, which means the load regulation is strictly related to the $V_{FB(AVG)}$. Also the lin e re gulation is r elated to th e $V_{FB(AVG)}$,if o ne wants to gets a bett er load or line regulation, a lower Vra mp is suggested once it meets equation 9.

For PWM operation, V $_{FB(AVG)}$ value can be deduced from equation 15.

$$V_{FB(AVG)} = V_{REF} + \frac{1}{2}\frac{V_{RAMP}}{R} \times \frac{R_1 // R_2}{_1 // R_2 + R_9} \quad (15)$$

Usually, R9 is set to 0 Ω, and it can also be set following equation 16 for a better no ise immunity. It should also set to be 5 timers smaller than R1//R2 to minimize its influence on Vramp.

$$R_9 \leq \frac{1}{2\pi \times C_4 \times 2F_{SW}} \quad (16)$$

Using equation 14 to calculate the o utput voltage can be complicated. To simplify the calculation of R1 in equat ion 14, a D C-blocking capacitor C dc can be added to filter the DC influ ence from R4 and R9. F igure 12 shows a simplified circuit with external ramp compen sation and a DC-blocking capacitor. With this ca pacitor, R1 can easily be obtained by using equ ation 17 for PWM mode operation.

$$R_{12} = \frac{(V_{OUT} - V_{REF} - \frac{1}{2}V_{RAMP})}{V_{REF} + \frac{1}{2}V_{RAMP}} R \qquad (17)$$

Cdc is sugg ested to be at least 10 times larger than C4 for better DC blocking perfo rmance, and should also not larger than 0.47 µF considerin g start up performance. In case one wants to use larger Cdc for a bet ter FB noise immunity, combined with reduced R1 and R2 to limit th e Cdc in a re asonable va lue without affecting the system start up. Be noted that even when the Cdc is applied, the load and line regulation are still Vramp related.
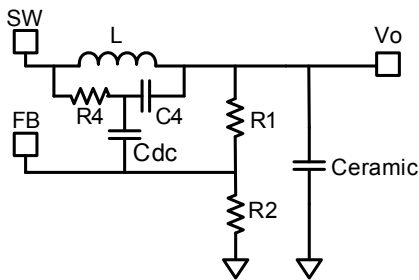

Figure 11—Simplified Circuit of Ceramic Capacitor with DC blocking capacitor

Input Capacitor
The input current to the step-down converter is discontinuous. Therefor e, a capacit or is require d to supply t he AC current to the step-down converter while maintaining the DC input voltage. Ceramic ca pacitors are recommen ded for best performance. In the layout, it's recommended to put the inpu t capacitors as close to t he IN pin as possible.

The capa citance va ries significantly over temperature. Capacitors with X5R and X7R ceramic die lectrics are recommen ded because they are fairly stable over temperature.

The capacit ors must also have a ripple current rating great er than the maxi mum input ripple current of th e converter. The input r ipple curren t can be estimated as follows:

$$I_{CIN} = I_{OUT} \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \qquad (18)$$

The worst-case conditio n occurs at V$_{IN}$ = 2V$_{OUT}$, where:

$$I_{CIN} = \frac{I_{OUT}}{2} \qquad (19)$$

For simplification, cho ose the in put capacit or whose RMS current rating is greate r than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If there is inp ut voltage ripple requirement in the sy stem design, choose the input capacitor that meets th e specification

The input voltage ripp le can be estimated a s follows:

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \qquad (20)$$

The worst-case condition occurs at V$_{IN}$ = 2V$_{OUT}$, where:

$$\Delta V_{IN} = \frac{1}{4F_{SW} \times C_{IN}} \times I_{OUT} \qquad (21)$$

Output Capacitor

The output capacitor is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The o utput voltage ripple can be estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 F_{SW} \times C_{OUT}}) \qquad (22)$$

In the case of ceramic capacitors, th e impedance at the switching frequency is domi nated by th e capacitance. The outpu t voltage rip ple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8F_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \qquad (23)$$

The output voltage ripple caused by ESR is very small. Therefore, an external ramp is needed to stabilize the system. Th e external ramp can be generated through resistor R4 and capacitor C4 following equation 5, 8 and 9.

In the case of POSCAP capacitor s, the ESR dominates the impedance at t he switching frequency. The ramp voltage gene rated from the ESR is high enough t o stabilize the system. Therefore, an external ramp is n ot needed. A minimum ESR value around 12m Ω is required to ensure sta ble operation of the converter. For

simplification, the output ripple can be approximated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (24)$$

Inductor

The inductor is required to supply constant current to the output load while being driven by the switching input voltage. A larger value inductor will result in less ripple current that will result in lower output ripple voltage. However, a larger value inductor will have a larger physical size, higher series resistance, and/or lower saturation current. A good rule for determining the inductor value is to allow the peak-to-peak ripple current in the inductor to be approximately 30~40% of the maximum switch current limit. Also, make sure that the peak inductor current is

below the maximum switch current limit. The inductance value can be calculated as:

$$L = \frac{V_{OUT}}{F_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (25)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current. The peak inductor current can be calculated as:

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (26)$$

The inductors listed in Table 1 are highly recommended for the high efficiency they can provide.

Table 1—Inductor Selection Guide

Part Number	Manufacturer	Inductance (µH)	DCR (mΩ)	Current Rating (A)	Dimensions L x W x H (mm³)	Switching Frequency (kHz)
PCMC-135T-R68MF	Cyntec	0.68	1.7	34	13.5 x 12.6 x 4.8	600
FDA1254-1R0M	TOKO	1	2	25.2	13.5 x 12.6 x 5.4	300~600
FDA1254-1R2M	TOKO	1.2	2.05	20.2	13.5 x 12.6 x 5.4	300~600

Typical Design Parameter Tables

The following tables include recommended component values for typical output voltages (1.2V, 2.5V, 3.3V) and switching frequencies (300kHz, 500kHz, and 700kHz). Refer to Tables 2-4 for design cases without external ramp compensation and Tables 5-7 for design cases with external ramp compensation. External ramp is not needed when high-ESR capacitors, such as electrolytic or POSCAPs are used. External ramp is needed when low-ESR capacitors, such as ceramic capacitors are used. For cases not listed in this datasheet, a calculator in excel spreadsheet can also be requested through a local sales representative to assist with the calculation.

Table 2—300kHz, 12V$_{IN}$

V$_{OUT}$ (V)	L (µH)	R1 (kΩ)	R2 (kΩ)	R7 (kΩ)
1.2	2.2	12.1	26.1	750
2.5	2.2	30	14.3	1500
3.3	1	40.2	13.3	1600

Table 3—500kHz, 12V$_{IN}$

V$_{OUT}$ (V)	L (µH)	R1 (kΩ)	R2 (kΩ)	R7 (kΩ)
1.2	1	12.1	26.1	442
2.5	1	30	14.3	845
3.3	1	40.2	13.3	1000

Table 4—700kHz, 12V$_{IN}$

V$_{OUT}$ (V)	L (µH)	R1 (kΩ)	R2 (kΩ)	R7 (kΩ)
1.2	1	12.1	26.1	316
2.5	1	30	14.3	590
3.3	1	40.2	13.3	806

Table 5—300kHz, 12V$_{IN}$

V$_{OUT}$ (V)	L (µH)	R1 (kΩ)	R2 (kΩ)	R4 (kΩ)	C4 (pF)	R7 (kΩ)
1.2	2.2	12.1	26.1	330	220	750
2.5	2.2	30	14.3	402	220	1500
3.3	2.2	40.2	12.4	422	220	1600

Table 6—500kHz, 12V$_{IN}$

V$_{OUT}$ (V)	L (μH)	R1 (kΩ)	R2 (kΩ)	R4 (kΩ)	C4 (pF)	R7 (kΩ)
1.2	1	12.1	26.1	374	220	442
2.5	1	30	14.3	412	220	845
3.3	1	40.2	12.4	422	220	1000

Table 7—700kHz, 12V$_{IN}$

V$_{OUT}$ (V)	L (μH)	R1 (kΩ)	R2 (kΩ)	R4 (kΩ)	C4 (pF)	R7 (kΩ)
1.2	1	12.1	26.1	240	220	316
2.5	1	30	14.3	412	220	590
3.3	1	40.2	12.4	422	220	806

TYPICAL APPLICATION
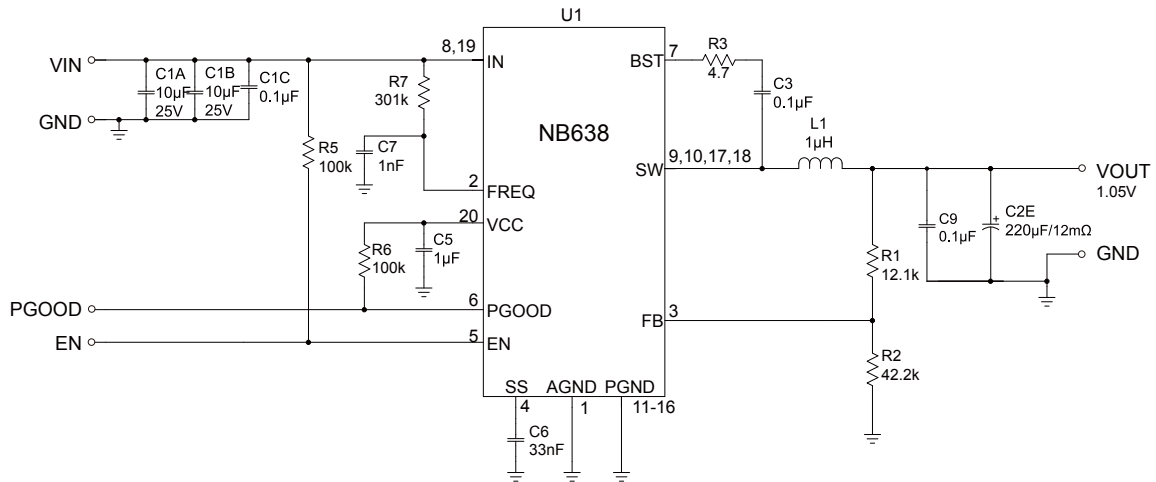
Figure 12 — Typical Application Circuit with No External Ramp
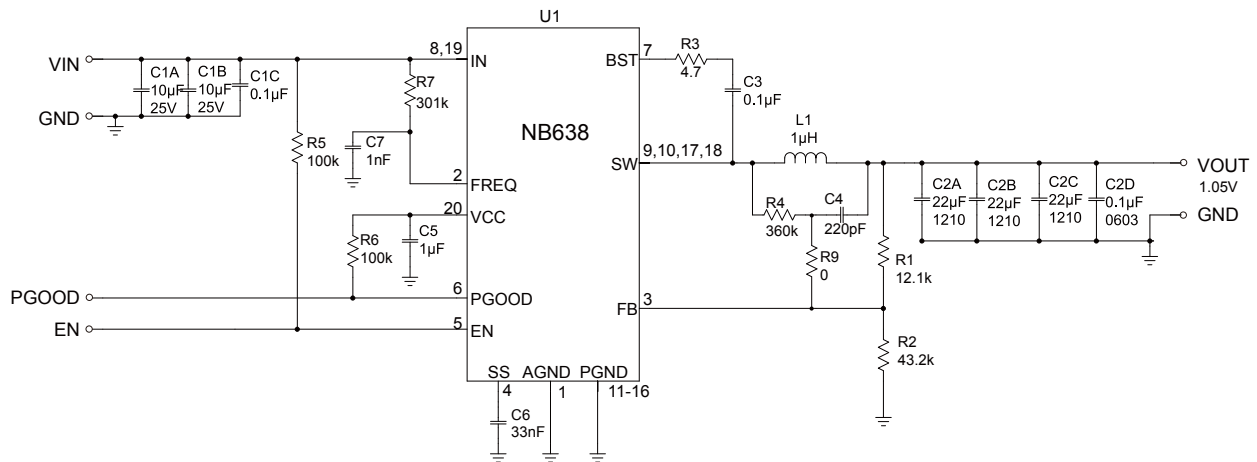
Figure 13 — Typical Application Circuit with Low ESR Ceramic Capacitor
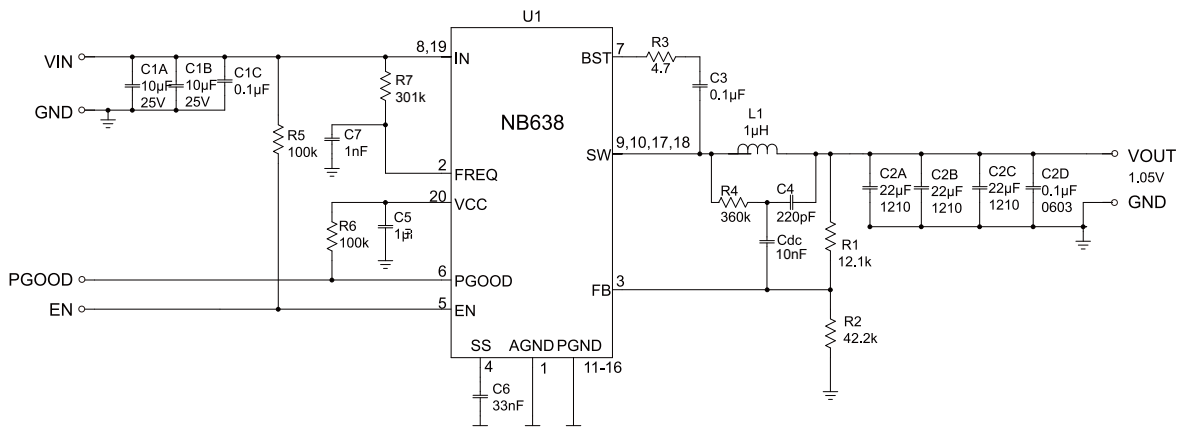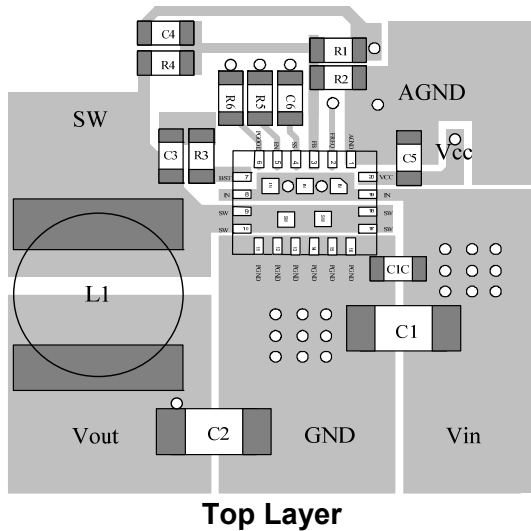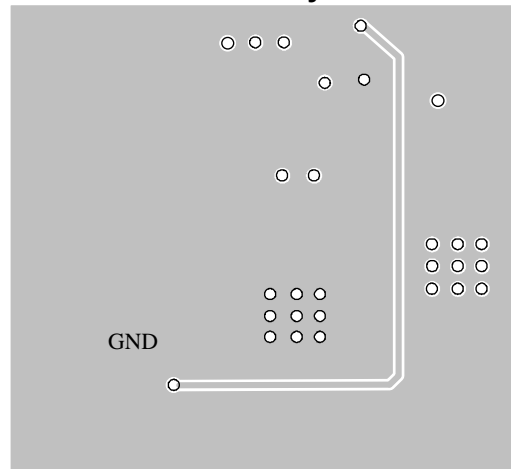
Figure 14 — Typical Application Circuit with Low ESR Ceramic Capacitor

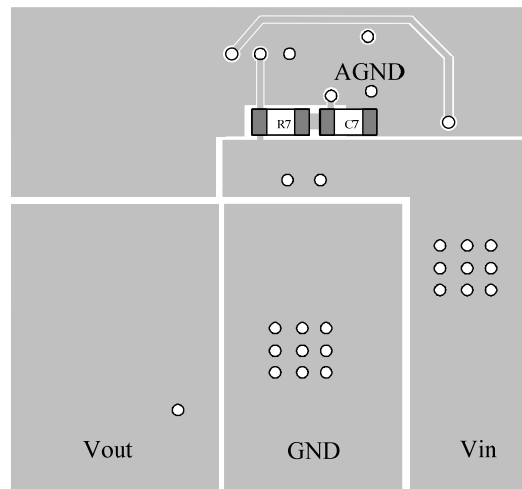**and DC-Blocking Capacitor**.

LAYOUT RECOMMENDATION

1. The high current paths (GND, IN,   and SW) should be   placed very close   to t he device with short, direct and wide traces.

2. Put the input capacitor s as close   to the I N and GND pins as possible.

3. Put the decoupling cap acitor as close to the V_{CC} and GND pins as possible.

4. Keep the switching no de SW short and away from the feedback network.

5. The external feedback resistor   s should be placed next to the FB pin. Make   sure that there is no via on the FB trace.

6. Keep the B ST voltage   path (BST,   C3, and SW) as short as possible.

7. Keep the bo ttom IN and SW pads c onnected with large copper to achieve better thermal performance.

8. Four-layer layout is strongly recommended to achieve better thermal performance.
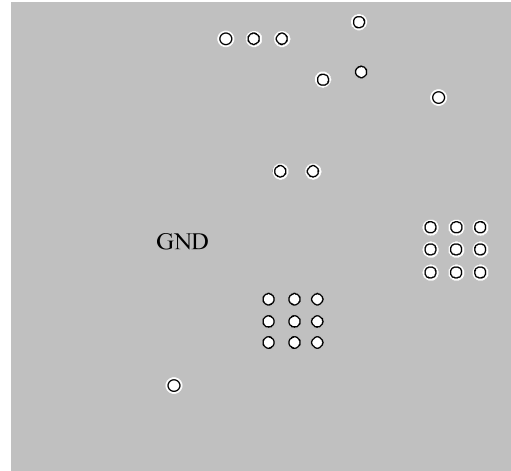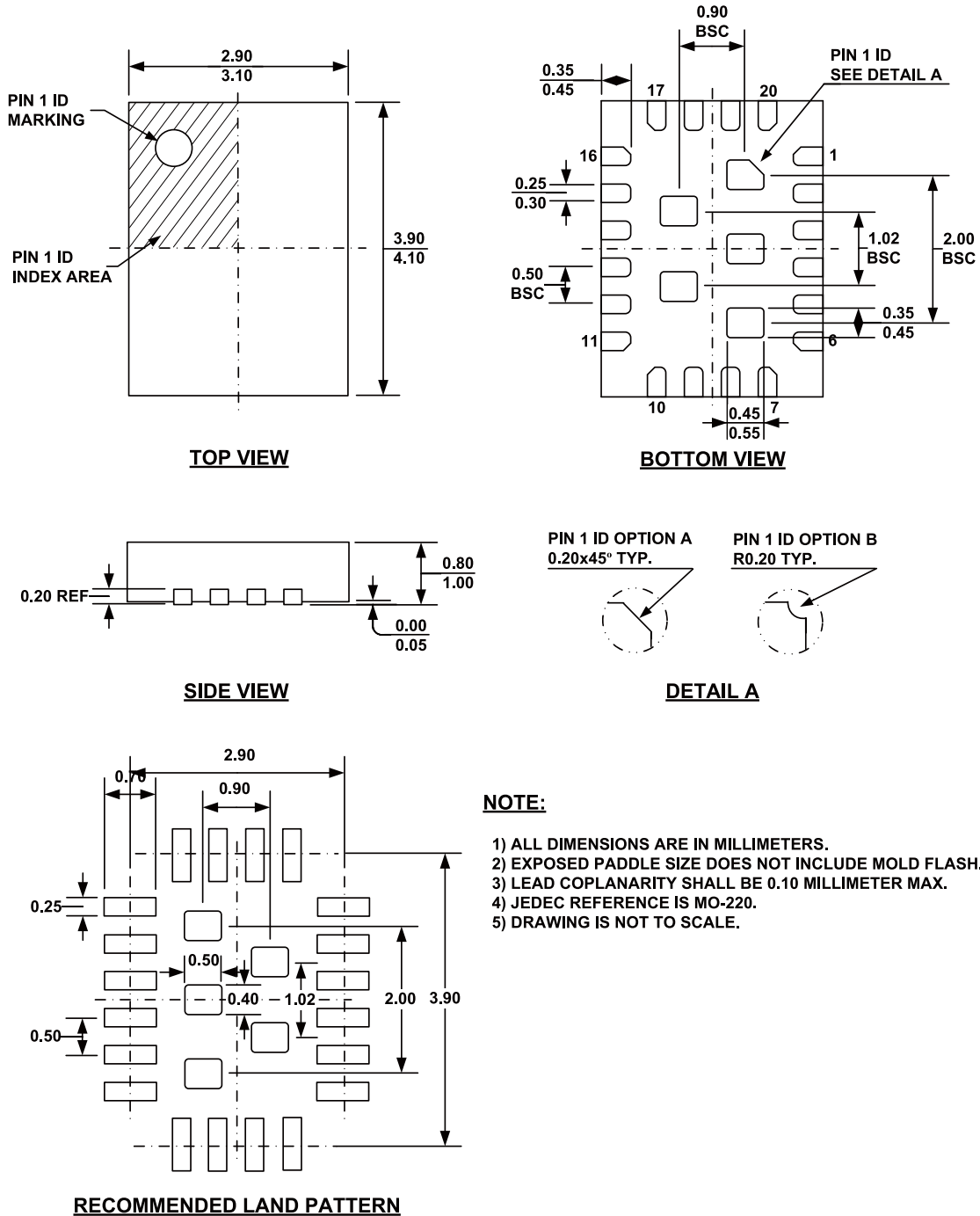

Inner1 Layer

Inner2 Layer

Top Layer

Bottom Layer

Figure 15—PCB Layout

PACKAGE INFORMATION

QFN20 (3x4mm)

TOP VIEW

BOTTOM VIEW

SIDE VIEW

DETAIL A

PIN 1 ID OPTION A
0.20x45º TYP.

PIN 1 ID OPTION B
R0.20 TYP.

RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.